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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Frank Chau Esq
F Chau & Associates LLP
1900 Hempstead Turnpike
Suite 501
East Meadow, NY 11554

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/492,544	GSCHWIND, MICHAEL K.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4 5, 10, 11, 31, 34, and 35 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Katzman, US Patent 3,737,871.

4. The rejections to claims 1, 4 5, 10, 11, 31, 34, and 35 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 3, mailed on October 1, 2003.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3, 32, 33, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, US Patent 3,737,871, in view of Morris, US Patent 6,286,095.

7. Claims 6, 8, 9, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, US Patent 3,737,871, in view of Wing, US Patent 5,926,832.

8. Claims 7, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman, US Patent 3,737,871, in view of Wing, US Patent 5,926,832, and Morris US Patent 6,286,095.

9. The rejections with respect to claims 2, 3, 6, 7, 8, 9, 32, 33, 36, 37, 38, 39 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 3, mailed on October 1, 2003.

10. Claims 12-19 and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al., US Patent 5953741 and Katzman, US Patent 3,737,871, cited as a prior art reference in the last office action, paper number 3, mailed on October 1, 2003.

11. Referring to claim 12, Veloy et al. in combination with Katzman have taught a method for renaming memory references to stack locations in a computer processing system, comprising the steps of

a. determining whether a load instruction references a location in a local stack using an architecturally defined register for accessing a stack location (Katzman, column 4, lines 5-25, Column 4, line 35, column 6, line 22, column 4, line 35, column 6, lines 22-47);

b. determining whether a rename register exists for the referenced location in the local stack, when the load instruction references the location using the architecturally defined register (Katzman, Abstract, column 1, lines 20-30, column 4, lines 36-67, column 4, line 35, column 4, lines 22-47); and

c. replacing the reference to the location by a reference to the rename register, when the rename register exists (Katzman, column 4, lines 36-67, column 4, line 35, column 4, lines 22-47).

12. Katzman has not specifically taught that this method for renaming memory references to stack locations is in a multiprocessor computer processing system wherein each processor comprises a respective local stack. However, Evoy et al. have taught a method for renaming memory references to stack locations in a multiprocessor computer processing system wherein each processor comprises a local stack. (column 4, lines 53-60, column 5, lines 2-27column 5, line 60-column 6, line 14, column 7, lines 26-33, Each stack based processor contains a local stack, see Figure 2, elements 78 and 76.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Evoy et al., include the steps of Katzman, as described above, in order to implement the TOS registers of Katzman, in each stack based processor of Veloy et al. for the desirable purpose of allowing the stack based processors of Veloy et al. to be operated at a maximum speed (Katzman, column 1, lines 20-30).

13. Referring to claim 13, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and wherein the architecturally defined register corresponds to a pointer for accessing stack locations (Katzman, Abstract, column 1, lines 20-30, column 4, lines 36-67).

14. Referring to claim 14, Katzman and Veloy et al. have taught the method according to claim 13, as described above, and wherein the pointer for accessing the stack locations is one of a stack pointer, a frame pointer, and an argument pointer (Katzman, column 3, lines 24-39, column 4, lines 42-48).

15. Referring to claim 15, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and wherein the architecturally defined stack access methods comprise push, pop, and other stack manipulation operations (Katzman, column 4, lines 33-36, column 7, lines 30-41).

16. Referring to claim 16, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and wherein said step of determining whether the renaming register exists comprises the step of computing one of a symbolic address and an actual address of the location (Katzman, Column 3, lines 55-67, Column 4, line 35, column 6, line 22).

17. Referring to claim 17, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and wherein said step of determining whether the rename register exists is performed during one of a decode, an address generation, and a memory access phase (Katzman, Column 3, lines 55-67, Column 4, line 35, column 6, line 22).

18. Referring to claim 18, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and further comprising the step of performing the load instruction from one of a main memory and a cache of the system, when the rename register does not exist (Katzman, Column 3, lines 55-67, Column 4, line 35, column 6, line 22, column 4, line 35, column 4, lines 22-47).

19. Referring to claim 19, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and further comprising the step of determining whether the load instruction references a location in any stack, including the local stack, using another register, when the load instruction does not reference the location using the architecturally defined register (Katzman, column 4, line 35, column 4, lines 22-47).

20. Referring to claim 21, Katzman and Veloy et al. have taught the method according to claim 19, as described above, and further comprising the step of performing the load instruction from one of a main memory and a cache of the system, when the load instruction does not reference the location using the other register (Katzman, column 6, lines 47-67).

21. Referring to claim 22, Katzman and Veloy et al. have taught the method according to claim 19, as described above, and further comprising the step of executing a consistency-preserving mechanism to perform the load instruction from the stack area, when the load instruction references the location using the other register (Katzman, column 4, line 35, column 4, lines 22-47).

22. Referring to claim 23, Katzman and Veloy et al. have taught the method according to claim 12, as described above, and further comprising the step of allocating a rename register for the location, when the rename register does not exist (Katzman, column 4, lines 36-67, Column 4, line 35, column 6, line 22).

23. Referring to claim 24, Katzman and Veloy et al. have taught the method according to claim 23, as described above, and further comprising the step of inserting an operation, into an instruction stream containing the load instruction, to load the location from a processor of the system to the allocated rename register, upon allocating the rename register (Katzman, column 7, lines 1-29, The operations inserted into the system to perform register renaming.).

24. Referring to claim 25, Katzman and Veloy et al. have taught the method according to claim 24, as described above, and further comprising the step of:

a. replacing the reference to the location by a reference to the allocated rename register, upon inserting the operation (Katzman, column 7, lines 1-29).

25. Referring to claim 26, Katzman has taught a method for renaming memory references to stack locations in a computer processing system, comprising the steps of:

a. determining whether a store instruction references a location in a local stack using an architecturally defined register for accessing a stack location (Katzman, column 4, lines 1-25, Abstract, column 1, lines 20-30, column 4, lines 36-67, Column 4, line 35, column 6, line 22, column 4, line 35, column 4, lines 22-47);

b. allocating a rename register for the location, when the store instruction references the location using the architecturally defined register (Katzman, column 4, lines 36-67, Column 4, line 35, column 6, line 22, column 4, line 35, column 4, lines 22-47); and

c. replacing the reference to the location by a reference to the rename register (Katzman, column 4, lines 36-67, Column 4, line 35, column 6, line 22, column 4, line 35, column 4, lines 22-47).

26. Katzman has not specifically taught that this method for renaming memory references to stack locations is in a multiprocessor computer processing system wherein each processor comprises a respective local stack. However, Evoy et al. have taught a method for renaming memory references to stack locations in a multiprocessor computer processing system wherein each processor comprises a local stack. (column 4, lines 53-60, column 5, lines 2-27column 5, line 60-column 6, line 14, column 7, lines 26-33, Each stack based processor contains a local stack, see Figure 2, elements 78 and 76.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Evoy et al., include the steps of Katzman, as described above, in order to implement the TOS registers of Katzman, in each

stack based processor of Veloy et al. for the desirable purpose of allowing the stack based processors of Veloy et al. to be operated at a maximum speed (Katzman, column 1, lines 20-30).

27. Referring to claim 27, Katzman and Evoy et al. have taught the method according to claim 26, further comprising the step of inserting an operation, into an instruction stream containing the store instruction, to store the location from the rename register to a main memory of the system, upon replacing the reference to the location by the reference to the rename register (Katzman, column 7, lines 1-29, Column 4, line 35, column 6, line 22, The operations inserted into the system to perform register renaming.).

28. Claim 28 does not recite limitations above the claimed invention set forth in claim 19 and is therefore rejected for the same reasons set forth in the rejection of claim 19 above.

29. Claim 29 does not recite limitations above the claimed invention set forth in claim 21 and is therefore rejected for the same reasons set forth in the rejection of claim 21 above.

30. Claim 30 does not recite limitations above the claimed invention set forth in claim 22 and is therefore rejected for the same reasons set forth in the rejection of claim 22 above.

31. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy et al. in view of Katzman, US Patent 3,737,871, in the last office action, paper number 3, mailed on October 1, 2003, and Wing et al., US Patent 5,926,832, in the last office action, paper number 3, mailed on October 1, 2003.

32. Referring to claim 20, Katzman has taught the method according to claim 19. Katzman has not taught wherein said step of determining whether the load instruction references the location using the other register comprises the step of marking translation lookaside buffer (TLB) entries of pages in the local stack as containing stack references, when the load instruction

references the location using the other register. However, Wing et al. have taught wherein said step of determining whether the load instruction references the location using the other register comprises the step of marking translation lookaside buffer (TLB) entries of pages in the local stack as containing stack references, when the load instruction references the location using the other register (Wing et al., column 22, lines 29-45, column 23, lines 2-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Katzman, utilize the translation lookaside buffer, as taught by Wing et al., as it's an easy way to keep track of stack references.

Response to Arguments

33. Applicant's arguments filed January 7, 2003 with respect to claims 12-30 are moot in view of the new grounds of rejection.

34. Applicant's arguments filed January 7, 2003 with respect to claims 1-11 and 31-39 have been fully considered but they are not persuasive.

35. On pages 12 and 13, Applicant argues in essence:

> *"Katzman does not teach "replacing the stack references with references to processor-internal registers" as claimed in claims 1 and 31, ...Katzman does not teach references to processor-internal registers or local stacks, essentially as claimed in claims 1 and 39."*
>
> However in Katzman what used to be an access to a memory stack (abstract, core memory, column 1, lines 20-30) now becomes an access to a processor-internal register (abstract, column 1 lines 20-30, column 1, lines 60-column 2, line 30, see TOS registers, column 3, lines 2-5). Therefore, Katzman has in fact taught replacing the stack references with references to processor-internal registers (The access to core stack

memory is replaced with an access to a processor internal register.). Therefore this argument is moot.

36. On page 13, Applicant argues in essence:

"The memory devices of Katzman, i.e., core memory and discs, are not analogous to processor-internal registers or local stacks. Katzman does not teach the architecture of the CPU, much less that the CPU comprises registers or stacks."

Applicant is correct in that the core memory and disks are not analogous to the processor-internal registers. The processor-internal registers are the TOS registers in Katzman (Figure 3, elements TR0-TR3, column 3, lines 2-5). However, a segment of the core memory is the stack (column 1, lines 20-30). Therefore this argument is moot.

37. On pages 13 and 14, Applicant argues in essence:

"Katzman does not teach an alternative to using the three registers. Katzman does not teach "determining that the rename register does not exist; and performing the load instruction from one of a main memory and a cache of the system" as claimed in claim 18. Katzman's method does not function without the three registers and does not teach performing the load instruction from one of a main memory and a cache pf the system" as claimed in claim 18, Therefore Katzman fails to teach all of the limitations of claim 18."

However, Katzman has in fact taught determining that the rename register does not exist (Column 5, lines 4-16, When SR=0 the rename register does not exist and the POP operation acts as if the TOS register are not present.). In Katzman, when the Load, or POP, operation is being performed with SR having a zero value the POP operation is performed as if the TOS registers are not present, i.e. from the core stack memory segment (column 1, lines 20-30). Therefore this argument is moot.

38. On page 14, Applicant argues in essence:

"Katzman does not teach inserting in-order write operations for all of the stack references that are write stack references, essentially as claimed in claims 3 and 33. Katzman merely teaches a naming scheme for top of stack registers."

Applicant is correct in that Katzman does not teach "*inserting in-order write operations for all of the stack references that are write stack references*" essentially as claimed in claims 3 and 33, as Morris has been cited for this teaching. See pages 8 and 9 in the last office action, paper number 3, mailed on October 1, 2003.

39. On pages 14 and 15, Applicant argues in essence:

"Morris does not teach inserting in-order write operations, essentially as claimed in claims 3 and 33. Morris teaches methods for performing a variety of operations (see column 6, lines 11=15). However, Morris does not teach or suggest targeting write stack references, much less, inserting in-order write operations for all of the stack references that are write stack references, essentially as claimed in claims 3 and 33."

However, Morris has in fact taught inserting in-order write operations (Abstract, Figures 4A, 4B, 11 and 12, column 4, lines 9-37, column 6, lines 62-67) for the desirable purpose of only operating on valid data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Katzman, insert in-order write operations as taught by Morris, such that the step of synchronizing an architected state between the processor-internal registers and a main memory of the computer processing system comprises the step of inserting in-order write operations for all of the stack references that are write stack references, for the desirable purpose of only operating on valid stack data. Therefore this argument is moot.

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER